ABSTRACT

The present invention provides an annealed wafer which has a wafer surface layer serving as a device fabricating region and having an excellent oxide film dielectric breakdown characteristic, and a wafer bulk layer in which oxide precipitates are present at a high density at the stage before the wafer is loaded into the device fabrication processes to give an excellent IG capability, and a method for manufacturing the annealed wafer. The present invention is directed to an annealed wafer obtained by performing heat treatment on a silicon wafer manufactured from a silicon single crystal grown by the Czochralski method, wherein a good chip yield of an oxide film dielectric breakdown characteristic in a region having at least a depth of up to 5 μm from a wafer surface is 95% or more, and a density of oxide precipitates detectable in the wafer bulk and each having a size not smaller than a size showing a gettering capability is not less than $1 \times 10^9/cm^3$.